

CLAIMS:

What is claimed is:

Sub B 1. A method of managing a network switch having a processor card
2 including a memory and a processing unit in the processor card
3 comprising:

4 detecting an error;

5 determining a type of the error;

6 determining whether a threshold has been reached; and,

7 performing a hitless rebuild in the processor card when the
8 type of the error is in a first set of errors and the threshold
9 has not been reached.

10 2. The method of claim 1, wherein the step of performing the
11 hitless rebuild includes:

12 performing an initialization of the memory; and,

13 protecting a portion of the memory from access by the
14 processing unit during the initialization.
15

1 3. The method of claim 1, wherein performing a hitless rebuild
2 includes protecting a portion of the memory that contains a set of
3 routing tables.

1 4. The method of claim 1, wherein performing a hitless rebuild
2 includes protecting a portion of the memory that contains a set of
3 state tables.

1 5. The method of claim 1, wherein the memory is accessed through
2 a set of memory addresses and performing a hitless rebuild
3 includes preventing the processing unit from accessing a
predetermined set of memory addresses in the set of memory
addresses.

6. The method of claim 1, wherein determining the type of the
error includes identifying a non-ignorable error.

1 7. The method of claim 1, further including setting the
2 processing unit to enter into a degraded mode when the type of the
3 error is in the first set of errors and the threshold has been
4 reached.

1 8. The method of claim 1, wherein determining whether the
2 threshold has been reached includes:

3 determining a number of hitless rebuilds that has been
4 performed in the processor card;

5 determining a time period from a first hitless rebuild time
6 and a second hitless rebuild time; and,

7 determining whether the number of hitless rebuilds versus the
8 time period has reached a ratio.

Sub B³ 9. An apparatus for managing a network switch having a processor
10 card including a memory and a processing unit in the processor
11 card comprising:

12 means for detecting an error;

13 means for determining a type of the error;

14 means for determining whether a threshold has been reached;

15 and,

16 means for performing a hitless rebuild in the processor card
17 when the type of the error is in a first set of errors and the
18 threshold has not been reached.

19 10. An article comprising a computer readable medium having
20 instructions stored thereon, which when executed, causes:

3 detection of an error;

4 determination of a type of the error;

5 determination of whether a threshold has been reached; and,

6 performance of a hitless rebuild in a processor card when the
7 type of the error is in a first set of errors and the threshold
8 has not been reached.

11. The article of claim 10, wherein the computer readable medium
further having instructions stored thereon, which when executed,
causes:

4 performance of an initialization of the memory; and,

5 protection of a portion of the memory from access by the
6 processing unit during the initialization.

12. The article of claim 10, wherein the computer readable medium
further having instructions stored thereon, which when executed,
causes:

4 performance of a hitless rebuild includes the step of
5 protecting a portion of the memory that contains a set of routing
6 tables.

1 13. The article of claim 10, wherein the computer readable medium
2 further having instructions stored thereon, which when executed,
3 causes:

4 protecting a portion of the memory that contains a set of
5 state tables.

1 14. The article of claim 10, wherein the memory is accessed
2 through a set of memory addresses and the computer readable medium
3 further having instructions stored thereon, which when executed,
4 causes:

5 prevention of a processing unit from accessing a
6 predetermined set of memory addresses in the set of memory
7 addresses.

1 15. The article of claim 10, wherein the computer readable medium
2 further having instructions stored thereon, which when executed,
3 causes:

4 identification of a non-ignorable error.

5 16. The article of claim 10, wherein the computer readable medium
2 further having instructions stored thereon, which when executed,
3 causes:

4 setting of the processing unit to enter into a degraded mode
5 when the type of the error is in the first set of errors and the
6 threshold has been reached.:

1 17. The article of claim 10, wherein the computer readable medium
2 further having instructions stored thereon, which when executed,
3 causes:

4 determination of a number of hitless rebuilds that has been
5 performed in the processor card;

6 determination of a time period from a first hitless rebuild
time and a second hitless rebuild time; and,

8 determination whether the number of hitless rebuilds versus
9 the time period has reached a ratio.

add B⁵ >

add C' >

add D' >